Atharva Shah

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OBJECTIVE

Seeking opportunities in the research and development of Mixed Signal and RF Integrated Circuits and Systems.

EDUCATION

University of California, San Diego **GPA: 3.913 (BS), 4.00 (MS/PhD)**
MS + PhD Electrical Engineering, Circuits and Systems, Advisor: Ian Galton –
BS Electrical Engineering, Circuits/Systems, Digital Signal Processing Dec. 2023

WORK EXPERIENCE

R&D RFIC Design Intern Jul 2024 - Sep 2024
Keysight Technologies – Research and Development Colorado Springs, CO

- Invention of a method to **linearize input capacitance** of Bipolar Transistor Differential Pairs
- Invention of a **tunable multi-band distortion cancellation** technique for high frequency differential transconductors
- Design, Layout, EMIR, SOA, RC extraction of a broadband active balun, utilizing a parasitic insensitive distortion cancellation technique to achieve **significant high frequency OIP3 improvements** over previous work.

FPGA / Digital Design Intern Jun 2023-Sep 2023
Lockheed Martin – Space Sunnyvale, CA

- Implemented algorithms in **Simulink** which were then transpiled to HDL using **HDL Coder**
- Designed an architecture for direct-write testing of LSRAM inside a **PolarFire FPGA** using Libero suite.
- Pipelined both SystemVerilog and Simulink designs in order to meet post-pnr timing requirements.

Electrical Engineering Intern Jun 2022-Aug 2022
West Coast Solutions Huntington Beach, CA

- Designed and laid out **100Ω diff-pair stripline** board for testing of Cameralink data.
- Developed **telemetry and power circuits** for a Turbo-Brayton cryocooler to be used in a NASA program.
- Designed a **power supply** circuit to distribute power for **op-amps, muxes, ADCs,** and **FPGA** core

PROJECTS

Integrated 2.5GHz Receiver Design: LNA + DnC + TIA (TSMC 65nm)

- LNA: 1.2 dB Noise Figure, with bias circuit providing 10mA $\pm$0.5% over PVT.
- DnC: Fully differential 50% duty cycle LO; IMR3 of 97 dB, IMR2 of 307 dB.
- TIA: Fully differential compensated 3-stage (incl. buffer) with CMFB and $f_u > 1.5$GHz

Fully Integrated 3-Level Buck Converter (PMICs) (gpdk 45nm)

- System and Transistor level design of a fully integrated 3-level buck converter at f_s=40MHz, η =0.91
- Analog blocks include: Error OTAs, Comparators, OpAmps, PWM generation
- Digital blocks include: cascoded level shifters, gate drivers, deadtime control

Digital OFDM Modem Design

- Implemented a **fully Digital OFDM modem + demodem** including cyclic prefix and **equalization**.
- Created digital **Phase Lock Loop (PLL)** and **Timing Recovery** implementations in MATLAB.
- Developed programs for QPSK equalization, I-Q balancing, and DC cancellation in MATLAB

8-bit Ladner-Fisher Adder Transistor Level Design (gpdk 45nm)

- Utilized odd-even PG network and increased critical path sizing to optimize design from 1.8GHz to 4.3GHz

Butler HTTP Server - `https://github.com/Shah06/butler`

- Wrote a **multithreaded web server** in Java, with NodeJS-esque syntax

TECHNICAL SKILLS (Keyword soup)

Equipment - Arbitrary Waveform Generator (AWG), BER Tester, Oscilloscope, VNA, Spectrum Analyzer, Function Generator, Keysight M8190A AWG, Keysight M8046A BERT
Languages - C, MATLAB, Simulink, Python, Verilog/SystemVerilog, C++, Java, ARM
Software - Cadence Virtuoso, Keysight ADS, Allegro, LTSpice, FPGA (Vivado, Libero, Quartus, ModelSim)
Process Nodes - ST 55nm SiGe BiCMOS, TSMC 65nm, IBM 180nm